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OPPENHEIMER WOLFF & DONNELLY
P. O. BOX 10356
PALO ALTO, CA 94303

EXAMINER
THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No. 09/373,014	**Applicant(s)** TSENG ET AL.
Office Action Summary	**Examiner** Kandasamy Thangavelu	**Art Unit** 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *10 June 2003* .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-22* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *11 August 1999* is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1.   This communication is in response to the Applicants' Amendment dated June 10,

2003. Claims 1-7, 9 and 11-16 were amended. Claims 1-122 of the application are

pending in the application. This office action is made non-final, in response to the

Request for Continued Examination.

Response to Amendments

2.   Applicant's arguments filed on June 10, 2003 have been fully considered. Claim

rejections under 35 U.S.C. 112 first and second paragraphs are withdrawn in response

to the applicant's amendments to the claims. New claim rejections under 35 USC

103(a) have been included in response to the amendments to the claims.

Drawings

3.   The draft person has objected to the drawings; see a copy of Form PTO-948 sent

with paper No. 5 for an explanation.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5.   The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness
        or nonobviousness.

6.   Claims 1, 2, 21, 3, 4, 7-13, 16-18 and 22 are rejected under 35 U.S.C. 103(a) as being

unpatentable over **Takahashi et al. (TA)** (U.S. Patent 6,061,283) in view of **Lin (LI)** (U.S.

Patent 6,421,251), and further in view of **Parulkar et al. (PA)** (U.S. Patent 6,363,509).

6.1   **TA** teaches semiconductor integrated circuit evaluation system. Specifically, as per

Claim 1, **TA** teaches a method of creating a record of a debug session for a software modeled

design on demand (CL4, L1-6; Fig 2A). **TA** does not expressly teach a method of creating a

record of a debug session for a hardware modeled design on demand. **LI** teaches a method of

creating a record of a debug session for a hardware modeled design on demand (CL3, L56-62;

CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-

39) and the user can accelerate the test/debug process by running the simulation through the

hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** with

the method of **LI** that included the method of creating a record of a debug session for a hardware

modeled design on demand, as the hardware modeled design would provide high speed and the

user could accelerate the test/debug process by running the simulation through the hardware

model of the circuit design.

   TA does not expressly teach selecting a simulation session range. **LI** teaches selecting a

simulation session range (CL13, L60-64), as the selected session range affects the simulation

speed since the system must spend time and resources to record the output data to the memory

(CL21, L9-15). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the method of **TA** with the method of **LI** that included

selecting a simulation session range, as the selected session range would affect the simulation

speed since the system must spend time and resources to record the output data to the memory.

   TA does not expressly teach selecting a simulation target range wherein the simulation

target range is within the simulation session range. **LI** teaches selecting a simulation target range

wherein the simulation target range is within the simulation session range (CL13, L64 to CL14,

L3), as the user can then perform analysis after simulation, by running the software simulation

with input logs to the hardware model to compute the value change dump of all hardware

components (CL42, L46-49). It would have been obvious to one of ordinary skill in the art at the

time of Applicants' invention to combine the method of **TA** with the method of **LI** that included

selecting a simulation target range wherein the simulation target range is within the simulation

session_range, as the user could then perform analysis after simulation, by running the software

simulation with input logs to the hardware model to compute the value change dump of all

hardware components.

TA teaches generating a Value change dump (VCD) file by dumping state information

from the software modeled design (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5,

L40-44; CL6, L21-25). TA does not expressly teach generating a Value change dump (VCD)

file by dumping state information from the hardware modeled design. LI teaches generating a

Value change dump (VCD) file by dumping state information from the hardware modeled design

(CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high

speed (CL3, L38-39) and the user can accelerate the test/debug process by running the

simulation through the hardware model of the circuit design (CL20, L24-26). It would have

been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine

the method of TA with the method of LI that included generating a Value change dump (VCD)

file by dumping state information from the hardware modeled design, as the hardware modeled

design would provide high speed and the user could accelerate the test/debug process by running

the simulation through the hardware model of the circuit design.

TA and LI do not expressly teach generating a Value change dump (VCD) file by

dumping state information for the selected simulation target range. PA teaches generating a

Value change dump (VCD) file by dumping state information for the selected simulation target

range (CL10, L21-38), as the simulation results of the simulation model can be used on a

physical implementation of the model to test it (CL10, L54-56) and as per TA, the IC evaluation

system can perform evaluation of the test patterns for testing the semiconductor device and the

functions of the semiconductor device (CL5, L58-62). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** and **LI**

with the method of **PA** that included generating a Value change dump (VCD) file by dumping

state information for the selected simulation target range, as the simulation results of the

simulation model could be used on a physical implementation of the model to test it and as per

TA, the IC evaluation system could perform evaluation of the test patterns for testing the

semiconductor device and the functions of the semiconductor.

Per claim 2: **TA** teaches accessing the VCD file directly from the beginning of the

simulation target range to debug the modeled design (CL2, L56-61; CL5, L36-46).

TA teaches recording primary inputs to the software modeled design for evaluation (CL2,

L54-60; CL1, L39-43). **TA** does not expressly teach recording primary inputs to the hardware

modeled design for evaluation. **LI** teaches recording primary inputs to the hardware modeled

design for evaluation (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled

design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by

running the simulation through the hardware model of the circuit design (CL20, L24-26). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

combine the method of **TA** with the method of **LI** that included recording primary inputs to the

hardware modeled design for evaluation, as the hardware modeled design would provide high

speed and the user could accelerate the test/debug process by running the simulation through the

hardware model of the circuit design.

TA teaches recording state information from the software modeled design (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not expressly recording state information from the hardware modeled design. LI teaches recording state information from the hardware modeled design (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by running the simulation through the hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of TA with the method of LI that included recording state information from the hardware modeled design, as the hardware modeled design would provide high speed and the user could accelerate the test/debug process by running the simulation through the hardware model of the circuit design.

TA does not expressly teach recording state information at the beginning of the simulation session range. PA teaches recording state information at the beginning of the simulation session range (CL10, L38-40), because as per LI the user can select a particular point at which the simulation is desired; then the user can select the start of session range which is recorded and simulate forward in time until the simulation reaches the desired point so the post simulation analysis point is reached fast (CL42, L23-45). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of TA with the method of PA that included recording state information at the beginning of the simulation session range, because the user could select a particular point at which the simulation is desired; then the user could select the start of session range which was recorded and simulate forward in

time until the simulation reached the desired point so the post simulation analysis point was

reached fast.

Per Claim 21: **TA** does not expressly teach that the simulation session range begins at a

simulation time t0 and ends at a simulation time t3. **LI** teaches that the simulation session range

begins at a simulation time t0 and ends at a simulation time t3 (CL13, L60-64), as the selected

session range affects the simulation speed since the system must spend time and resources to

record the output data to the memory (CL21, L9-15). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** with

the method of **LI** that included simulation session range beginning at a simulation time t0 and

ending at a simulation time t3, as the selected session range would affect the simulation speed

since the system must spend time and resources to record the output data to the memory.

TA does not expressly teach that the simulation target range begins at a simulation time

t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to

simulation time t0 and simulation time t2 is less than or equal to simulation time t3. **LI** teaches

that the simulation target range begins at a simulation time t1 and ends at a simulation time t2,

wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time

t2 is less than or equal to simulation time t3 (CL13, L64 to CL14, L3), as the user can then

perform analysis after simulation, by running the software simulation with input logs to the

hardware model to compute the value change dump of all hardware components (CL42, L46-49).

It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention

to combine the method of **TA** with the method of **LI** that included the simulation target range

beginning at a simulation time t1 and ending at a simulation time t2, wherein the simulation time

t1 was greater than or equal to simulation time t0 and simulation time t2 was less than or equal to

simulation time t3, as the user could then perform analysis after simulation, by running the

software simulation with input logs to the hardware model to compute the value change dump of

all hardware components.

Per Claim 3: **TA** teaches evaluating in the modeled design from simulation time t0 to

simulation time t2 (CL3, L39 to CL4, L26; CL1, L27-29; CL1, L34-35; CL3, L4-8; CL5, L34-

37).

TA teaches recording primary inputs to the software modeled design for evaluation (CL2,

L54-60; CL1, L39-43). **TA** does not expressly teach recording primary inputs to the hardware

modeled design for evaluation. **LI** teaches recording primary inputs to the hardware modeled

design for evaluation (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled

design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by

running the simulation through the hardware model of the circuit design (CL20, L24-26). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

combine the method of **TA** with the method of **LI** that included recording primary inputs to the

hardware modeled design for evaluation, as the hardware modeled design would provide high

speed and the user could accelerate the test/debug process by running the simulation through the

hardware model of the circuit design.

TA teaches recording state information from the software modeled design (CL2, L56-61;

CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly

recording state information from the hardware modeled design. **LI** teaches recording state

information from the hardware modeled design (CL3, L56-62; CL5, L34-40; CL18, L40-43), as

the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the

test/debug process by running the simulation through the hardware model of the circuit design

(CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the method of **TA** with the method of **LI** that included

recording state information from the hardware modeled design, as the hardware modeled design

would provide high speed and the user could accelerate the test/debug process by running the

simulation through the hardware model of the circuit design.

TA and LI do not expressly teach recording state information for a portion of the

simulation session range. **PA** teaches recording state information for a portion of the simulation

session range (CL10, L21-38), as the simulation results of the simulation model can be used on a

physical implementation of the model to test it (CL10, L54-56) and as per **TA**, the IC evaluation

system can perform evaluation of the test patterns for testing the semiconductor device and the

functions of the semiconductor device (CL5, L58-62). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** and **LI**

with the method of **PA** that included recording state information for a portion of the simulation

session range, as the simulation results of the simulation model could be used on a physical

implementation of the model to test it and as per **TA**, the IC evaluation system could perform

evaluation of the test patterns for testing the semiconductor device and the functions of the

semiconductor device.

Per Claim 4: **TA** teaches the step of generating the VCD file further comprises generating

evaluated results from the modeled design based on the recorded primary inputs and recorded

state information (CL4, L21-26; CL1, L27-29; CL1, L34-35; CL3, L4-8; CL5, L34-37; CL5,

L59-63).

TA teaches saving the evaluated results into the VCD file (CL4, L1-26; CL6, L21-36).

TA does not expressly teach saving the evaluated results of the simulation target range into the

VCD file. **PA** teaches saving the evaluated results of the simulation target range into the VCD

file (CL10, L21-38), as the simulation results of the simulation model can be used on a physical

implementation of the model to test it (CL10, L54-56) and as per **TA**, the IC evaluation system

can perform evaluation of the test patterns for testing the semiconductor device and the functions

of the semiconductor device (CL5, L58-62). It would have been obvious to one of ordinary skill

in the art at the time of Applicants' invention to combine the method of **TA** with the method of

PA that included saving the evaluated results of the simulation target range into the VCD file, as

the simulation results of the simulation model could be used on a physical implementation of the

model to test it and as per **TA**, the IC evaluation system could perform evaluation of the test

patterns for testing the semiconductor device and the functions of the semiconductor device.

Per Claim 7: **TA** teaches recording primary inputs (CL2, L54-60; CL1, L39-43).

Per Claim 8: **TA** teaches recording state information of the modeled design (CL2, L56-

61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly

teach saving state information of the modeled design at simulation time t0 in a first file and

saving state information of the modeled design at simulation time t3 in a second file. **PA** teaches

saving state information of the modeled design at simulation time t0 in a first file and saving

state information of the modeled design at simulation time t3 in a second file (CL10, L38-48),

because as per **LI** the user can select a particular point at which the simulation is desired; then

the user can select the start of session range which is recorded and simulate forward in time until

the simulation reaches the desired point so the post simulation analysis point is reached fast

(CL42, L23-45). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the method of **TA** with the method of **PA** that included saving

state information of the modeled design at simulation time t0 in a first file and saving state

information of the modeled design at simulation time t3 in a second file, because the user could

select a particular point at which the simulation is desired; then the user could select the start of

session range which was recorded and simulate forward in time until the simulation reached the

desired point so the post simulation analysis point was reached fast.

6.2   As per Claim 9, **TA** teaches an electronic design automation system for verifying a user

design (Fig 2A); comprising:

        a computing system including a central processing unit and memory for modeling the

user design in software (Fig. 2A; CL4, L67 to CL5, L46; CL1, L27-29); and

        an internal bus system coupled to the computing system (Fig 2A).

        TA teaches hardware logic coupled to the internal bus system and for modeling at least a

portion of the user design in hardware (Fig 2A, Item 22; CL3, L55-65). **TA** does not expressly

teach reconfigurable hardware logic coupled to the internal bus system and for modeling at least

a portion of the user design in hardware. **LI** teaches reconfigurable hardware logic coupled to

the internal bus system and for modeling at least a portion of the user design in hardware (CL18,

L40-43), as the reconfigurable hardware can be programmably configured to model the hardware

portion of the user's electronic system design (CL18, L40-43). It would have been obvious to

one of ordinary skill in the art at the time of Applicants' invention to combine the method of **TA**

with the method of **LI** that included reconfigurable hardware logic coupled to the internal bus

system and for modeling at least a portion of the user design in hardware, as the reconfigurable

hardware could be programmably configured to model the hardware portion of the user's

electronic system design.

TA does not expressly teach control logic coupled to the internal bus system for

controlling the delivery of data between the reconfigurable hardware logic and the computing

system. **LI** teaches control logic coupled to the internal bus system for controlling the delivery

of data between the reconfigurable hardware logic and the computing system (CL12, L51-61), as

the that allows the entire circuit design to be modeled in software and the evaluation components

to be modeled in hardware (CL12, L53-56), so the system can simulate the circuit in software for

a time period and then accelerate the simulation in hardware (CL13, L10-11). It would have

been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine

the method of **TA** with the method of **LI** that included control logic coupled to the internal bus

system for controlling the delivery of data between the reconfigurable hardware logic and the

computing system, as the that would allow the entire circuit design to be modeled in software

and the evaluation components to be modeled in hardware, so the system could simulate the

circuit in software for a time period and then accelerate the simulation in hardware.

TA teaches VCD on-demand logic for recording a selected simulation session (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not expressly teach VCD on-demand logic for recording at least a portion of a selected simulation session range. PA teaches VCD on-demand logic for recording at least a portion of a selected simulation session range (CL10, L21-38), as the simulation results of the simulation model can be used on a physical implementation of the model to test it (CL10, L54-56) and as per TA, the IC evaluation system can perform evaluation of the test patterns for testing the semiconductor device and the functions of the semiconductor device (CL5, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of TA with the method of PA that included VCD on-demand logic for recording at least a portion of a selected simulation session range, as the simulation results of the simulation model could be used on a physical implementation of the model to test it and as per TA, the IC evaluation system could perform evaluation of the test patterns for testing the semiconductor device and the functions of the semiconductor device.

TA teaches dumping state information from the software model into a VCD file (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not expressly teach dumping state information from the hardware model into a VCD file. LI teaches dumping state information from the hardware model into a VCD file (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by running the simulation through the hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of TA with the method of LI that

included dumping state information from the hardware model into a VCD file, as the hardware

modeled design would provide high speed and the user could accelerate the test/debug process

by running the simulation through the hardware model of the circuit design.

TA and LI do not expressly teach dumping state information for a selected simulation

target range, where the simulation target range is within the simulation session range. PA

teaches dumping state information for a selected simulation target range, where the simulation

target range is within the simulation session range (CL10, L21-38), as the simulation results of

the simulation model can be used on a physical implementation of the model to test it (CL10,

L54-56) and as per TA, the IC evaluation system can perform evaluation of the test patterns for

testing the semiconductor device and the functions of the semiconductor device (CL5, L58-62).

It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention

to combine the method of TA and LI with the method of PA that included dumping state

information for a selected simulation target range, where the simulation target range is within the

simulation session range, as the simulation results of the simulation model could be used on a

physical implementation of the model to test it and as per TA, the IC evaluation system could

perform evaluation of the test patterns for testing the semiconductor device and the functions of

the semiconductor device.

Per Claim 10: TA teaches access logic for accessing the VCD file directly from

simulation time tl to debug the user design (CL2, L56-61; CL5, L36-46).

TA does not expressly teach first range selection logic for selecting a simulation session

range which begins at a simulation time t0 and ends at a simulation time t3. LI teaches first

range selection logic for selecting a simulation session range which begins at a simulation time

t0 and ends at a simulation time t3 (CL13, L60-64), as the selected session range affects the

simulation speed since the system must spend time and resources to record the output data to the

memory (CL21, L9-15). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to combine the system of **TA** with the system of **LI** that included first

range selection logic for selecting a simulation session range which begins at a simulation time

t0 and ends at a simulation time t3, as the selected session range would affect the simulation

speed since the system must spend time and resources to record the output data to the memory.

TA does not expressly teach second range selection logic for selecting a simulation target

range which begins at a simulation time t1 and ends at a simulation time t2, wherein the

simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less

than or equal to simulation time t3. **LI** teaches second range selection logic for selecting a

simulation target range which begins at a simulation time t1 and ends at a simulation time t2,

wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time

t2 is less than or equal to simulation time t3 (CL13, L64 to CL14, L3), as the user can then

perform analysis after simulation, by running the software simulation with input logs to the

hardware model to compute the value change dump of all hardware components (CL42, L46-49).

It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention

to combine the system of **TA** with the system of **LI** that included second range selection logic

for selecting a simulation target range which began at a simulation time t1 and ended at a

simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0

and simulation time t2 is less than or equal to simulation time t3, as the user could then perform

analysis after simulation, by running the software simulation with input logs to the hardware

model to compute the value change dump of all hardware components.

TA teaches dump logic for generating a VCD file of the software-modeled design (CL2,

L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not

expressly teach dump logic for generating a VCD file of the hardware-modeled design. LI

teaches dump logic for generating a VCD file of the hardware-modeled design (CL3, L56-62;

CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-

39) and the user can accelerate the test/debug process by running the simulation through the

hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the system of TA with

the system of LI that included dump logic for generating a VCD file of the hardware-modeled

design, as the hardware modeled design would provide high speed and the user could accelerate

the test/debug process by running the simulation through the hardware model of the circuit

design.

TA and LI do not expressly teach dump logic for generating a VCD file for the selected

simulation target range. PA teaches dump logic for generating a VCD file for the selected

simulation target range (CL10, L21-38), as the simulation results of the simulation model can be

used on a physical implementation of the model to test it (CL10, L54-56) and as per TA, the IC

evaluation system can perform evaluation of the test patterns for testing the semiconductor

device and the functions of the semiconductor device (CL5, L58-62). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the

system of TA and LI with the system of PA that included dump logic for generating a VCD file

for the selected simulation target range, as the simulation results of the simulation model could

be used on a physical implementation of the model to test it and as per **TA**, the IC evaluation

system could perform evaluation of the test patterns for testing the semiconductor device and the

functions of the semiconductor device.

Per Claim 11: **TA** teaches that the VCD on-demand logic further comprises test bench

process for providing primary inputs to the hardware-modeled design for evaluation (CL1, L32-

33); and

recording logic in the computing system for recording data associated with at least one

parameter in the simulation session rang (CL6, L9-13; CL6, L21-25).

Per Claim 12: **TA** teaches that the VCD on-demand logic further comprises process logic

in the computing system for loading the recorded data associated with at least one parameter

(CL6, L21-27).

TA teaches evaluation logic in the hardware logic for evaluating in the

hardware-modeled design the primary inputs from simulation time t0 to simulation time t2 (Fig

2A, Item 22; CL3, L55-65; CL6, L30-36). **TA** does not expressly teach evaluation logic in the

reconfigurable hardware logic for evaluating in the hardware-modeled design the primary inputs

from simulation time t0 to simulation time t2. **LI** teaches evaluation logic in the reconfigurable

hardware logic for evaluating in the hardware-modeled design the primary inputs from

simulation time t0 to simulation time t2 (CL18, L40-43), as the reconfigurable hardware can be

programmably configured to model the hardware portion of the user's electronic system design

(CL18, L40-43). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with the system of **LI** that included evaluation logic in the reconfigurable hardware logic for evaluating in the hardware-modeled design the primary inputs from simulation time t0 to simulation time t2, as the reconfigurable hardware could be programmably configured to model the hardware portion of the user's electronic system design.

Per Claim 13: **TA** teaches the dump logic dumps the evaluated results from the software-modeled design based on the primary inputs during the simulation into the VCD file (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly teach the dump logic dumps the evaluated results from the hardware-modeled design based on the primary inputs during the simulation into the VCD file. **LI** teaches the dump logic dumps the evaluated results from the hardware-modeled design based on the primary inputs during the simulation into the VCD file (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by running the simulation through the hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with the system of **LI** that included the dump logic dumping the evaluated results from the hardware-modeled design based on the primary inputs during the simulation into the VCD file, as the hardware modeled design would provide high speed and the user could accelerate the test/debug process by running the simulation through the hardware model of the circuit design.

TA and LI do not expressly teach the dump logic dumps the evaluated results based on the primary inputs during the simulation target range into the VCD file. **PA** teaches the dump logic dumps the evaluated results based on the primary inputs during the simulation target range into the VCD file (CL10, L21-38), as the simulation results of the simulation model can be used on a physical implementation of the model to test it (CL10, L54-56) and as per **TA**, the IC evaluation system can perform evaluation of the test patterns for testing the semiconductor device and the functions of the semiconductor device (CL5, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** and **LI** with the system of **PA** that included the dump logic dumping the evaluated results based on the primary inputs during the simulation target range into the VCD file, as the simulation results of the simulation model could be used on a physical implementation of the model to test it and as per **TA**, the IC evaluation system could perform evaluation of the test patterns for testing the semiconductor device and the functions of the semiconductor device.

Per Claim 16: **TA** teaches write logic for writing the primary inputs (CL2, L54-60; CL1, L39-43).

TA teaches write logic for writing state information from the software model (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly write logic for writing state information from the hardware model. **LI** teaches write logic for writing state information from the hardware model (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by running the simulation through the hardware model of the circuit

design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to combine the system of **TA** with the system of **LI** that included write

logic for writing state information from the hardware model, as the hardware modeled design

would provide high speed and the user could accelerate the test/debug process by running the

simulation through the hardware model of the circuit design.

TA does not expressly teach write logic for writing state information at simulation time

t0. **PA** teaches write logic for writing state information at simulation time t0 (CL10, L38-40),

because as per **LI** the user can select a particular point at which the simulation is desired; then

the user can select the start of session range which is recorded and simulate forward in time until

the simulation reaches the desired point so the post simulation analysis point is reached fast

(CL42, L23-45). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the system of **TA** with the system of **PA** that included write

logic for writing state information at simulation time t0, because the user could select a particular

point at which the simulation was desired; then the user could select the start of session range

which was recorded and simulate forward in time until the simulation reached the desired point

so the post simulation analysis point was reached fast.

Per Claim 17: **TA** teaches state save logic for saving state information of the software

modeled design (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-

25). **TA** does not expressly teach state save logic for saving state information of the

hardware-modeled design. **LI** teaches state save logic for saving state information of the

hardware-modeled design (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled

design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by

running the simulation through the hardware model of the circuit design (CL20, L24-26). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

combine the system of **TA** with the system of **LI** that included state save logic for saving state

information of the hardware-modeled design, as the hardware modeled design would provide

high speed and the user could accelerate the test/debug process by running the simulation

through the hardware model of the circuit design.

TA does not expressly teach state save logic for saving state information at simulation

time t0 in a first file and saving state information at simulation time t3 in a second file. **PA**

teaches state save logic for saving state information at simulation time t0 in a first file and saving

state information at simulation time t3 in a second file (CL10, L38-48), because as per **TI** the

user can select a particular point at which the simulation is desired; then the user can select the

start of session range which is recorded and simulate forward in time until the simulation reaches

the desired point so the post simulation analysis point is reached fast (CL42, L23-45). It would

have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

combine the system of **TA** with the system of **PA** that included state save logic for saving state

information at simulation time t0 in a first file and saving state information at simulation time t3

in a second file, because the user could select a particular point at which the simulation is

desired; then the user could select the start of session range which was recorded and simulate

forward in time until the simulation reached the desired point so the post simulation analysis

point was reached fast.

6.3   As per Claim 18, **TA** teaches a VCD on-demand system for providing evaluated

information for selected simulation times, the evaluation occurring in a software model (CL2,

L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not

expressly teach a VCD on-demand system for providing evaluated information for selected

simulation times, the evaluation occurring in a hardware model. **LI** teaches a VCD on-demand

system for providing evaluated information for selected simulation times, the evaluation

occurring in a hardware model (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware

modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug

process by running the simulation through the hardware model of the circuit design (CL20, L24-

26). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to combine the system of **TA** with the system of **LI** that included a VCD on-demand

system for providing evaluated information for selected simulation times, the evaluation

occurring in a hardware model, as the hardware modeled design would provide high speed and

the user could accelerate the test/debug process by running the simulation through the hardware

model of the circuit design.

        TA and **LI** do not expressly teach a VCD on-demand system for providing evaluated

information for a selected simulation target range of simulation times. **PA** teaches a VCD

on-demand system for providing evaluated information for a selected simulation target range of

simulation times (CL10, L21-38), as the simulation results of the simulation model can be used

on a physical implementation of the model to test it (CL10, L54-56) and as per **TA**, the IC

evaluation system can perform evaluation of the test patterns for testing the semiconductor

device and the functions of the semiconductor device (CL5, L58-62). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the

system of **TA** and **LI** with the system of **PA** that included a VCD on-demand system for

providing evaluated information for a selected simulation target range of simulation times, as the

simulation results of the simulation model could be used on a physical implementation of the

model to test it and as per **TA**, the IC evaluation system could perform evaluation of the test

patterns for testing the semiconductor device and the functions of the semiconductor device.

TA does not expressly teach first logic for selecting a simulation session range. **LI**

teaches first logic for selecting a simulation session range (CL13, L60-64), as the selected

session range affects the simulation speed since the system must spend time and resources to

record the output data to the memory (CL21, L9-15). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with

the system of **LI** that included first logic for selecting a simulation session range, as the selected

session range would affect the simulation speed since the system must spend time and resources

to record the output data to the memory.

TA does not expressly teach second logic selecting a simulation target range, wherein the

simulation target range is within the simulation session range. **LI** teaches second logic selecting

a simulation target range, wherein the simulation target range is within the simulation session

range (CL13, L64 to CL14, L3), as the user can then perform analysis after simulation, by

running the software simulation with input logs to the hardware model to compute the value

change dump of all hardware components (CL42, L46-49). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with

the system of **LI** that included second logic selecting a simulation target range, wherein the

simulation target range is within the simulation session range, as the user could then perform

analysis after simulation, by running the software simulation with input logs to the hardware

model to compute the value change dump of all hardware components.

TA teaches generation logic for generating a VCD file of the evaluated information by

dumping state information from the software model (CL2, L56-61; CL1, L27-29; CL4, L5-6;

CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not expressly teach generation logic for

generating a VCD file of the evaluated information by dumping state information from the

hardware model. LI teaches generation logic for generating a VCD file of the evaluated

information by dumping state information from the hardware model (CL3, L56-62; CL5, L34-

40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the

user can accelerate the test/debug process by running the simulation through the hardware model

of the circuit design (CL20, L24-26). It would have been obvious to one of ordinary skill in the

art at the time of Applicants' invention to combine the system of TA with the system of LI that

included generation logic for generating a VCD file of the evaluated information by dumping

state information from the hardware model, as the hardware modeled design would provide high

speed and the user could accelerate the test/debug process by running the simulation through the

hardware model of the circuit design.

TA and LI do not expressly teach generation logic for generating a VCD file of the

evaluated information for the selected simulation target range by dumping state information. PA

teaches generation logic for generating a VCD file of the evaluated information for the selected

simulation target range by dumping state information (CL10, L21-38), as the simulation results

of the simulation model can be used on a physical implementation of the model to test it (CL10,

L54-56) and as per **TA**, the IC evaluation system can perform evaluation of the test patterns for testing the semiconductor device and the functions of the semiconductor device (CL5, L58-62). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** and **LI** with the system of **PA** that included generation logic for generating a VCD file of the evaluated information for the selected simulation target range by dumping state information, as the simulation results of the simulation model could be used on a physical implementation of the model to test it and as per **TA**, the IC evaluation system could perform evaluation of the test patterns for testing the semiconductor device and the functions of the semiconductor device.

Per Claim 22: This is a system claim having the same limitations as Claim 21. So Claim 22 is rejected based on the same reasoning as Claim 21, <u>supra.</u>

7.   Claims 5, 6, 14, 15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takahashi et al. (TA)** (U.S. Patent 6,061,283) in view of **Lin (LI)** (U.S. Patent 6,421,251) and **Parulkar et al. (PA)** (U.S. Patent 6,363,509), and further in view of **Matsumura et al. (MA)** (U.S. Patent 6,370,675).

7.1   As per Claim 5, **TA, LI** and **PA** teach the method of Claim 1. **TA, LI** and **PA** do not expressly teach compressing the primary inputs recording the compressed primary inputs. **MA** teaches compressing the primary inputs recording the compressed primary inputs (Abstract, L12-15; CL5, L55 to CL6, L10), as the test pattern data after compression is stored in the memory

(CL10, L54-56) and the memory required will be reduced by compression. It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the

method of **TA, LI** and **PA** with the method of **MPA** that included compressing the primary

inputs recording the compressed primary inputs, as the test pattern data after compression would

be stored in the memory and the memory required would be reduced by compression.

TA teaches recording state information from the software modeled design (CL2, L56-61;

CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly

recording state information from the hardware modeled design. **LI** teaches recording state

information from the hardware modeled design (CL3, L56-62; CL5, L34-40; CL18, L40-43), as

the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the

test/debug process by running the simulation through the hardware model of the circuit design

(CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the method of **TA** with the method of **LI** that included

recording state information from the hardware modeled design, as the hardware modeled design

would provide high speed and the user could accelerate the test/debug process by running the

simulation through the hardware model of the circuit design.

TA does not expressly teach recording state information at the start of the simulation

session range. **PA** teaches recording state information at the start of the simulation session range

(CL10, L38-40), because as per **LI** the user can select a particular point at which the simulation

is desired; then the user can select the start of session range which is recorded and simulate

forward in time until the simulation reaches the desired point so the post simulation analysis

point is reached fast (CL42, L23-45). It would have been obvious to one of ordinary skill in the

art at the time of Applicants' invention to combine the method of **TA** with the method of **PA** that

included recording state information at the start of the simulation session range, because the user

could select a particular point at which the simulation was desired; then the user could select the

start of session range which was recorded and simulate forward in time until the simulation

reached the desired point so the post simulation analysis point was reached fast.

Per Claim 6: **TA** teaches decompressing the compressed primary inputs (CL2, L29-31);

and

providing the decompressed primary inputs to the modeled design for evaluation (CL1,

L32-33; CL2, L31-33; Fig. 1, Blk 17, 10 and 11).

7.2   As per Claim 14, **TA, LI** and **PA** teach the system of Claim 13. **TA, LI** and **PA** do not

expressly teach compression logic for compressing the primary inputs and write logic for writing

the compressed primary inputs. **MA** teaches compression logic for compressing the primary

inputs and write logic for writing the compressed primary inputs (Abstract, L12-15; CL5, L55 to

CL6, L10), as the test pattern data after compression is stored in the memory (CL10, L54-56)

and the memory required will be reduced by compression. It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the system of **TA, LI** and

PA with the system of **MA** that included compression logic for compressing the primary inputs

and write logic for writing the compressed primary inputs, as the test pattern data after

compression would be stored in the memory and the memory required would be reduced by

compression.

TA teaches write logic for writing state information from the software model (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not expressly write logic for writing state information from the hardware model. **LI** teaches write logic for writing state information from the hardware model (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by running the simulation through the hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with the system of **LI** that included write logic for writing state information from the hardware model, as the hardware modeled design would provide high speed and the user could accelerate the test/debug process by running the simulation through the hardware model of the circuit design.

TA does not expressly teach write logic for writing state information at simulation time t0. **PA** teaches write logic for writing state information at simulation time t0 (CL10, L38-40), because as per **LI** the user can select a particular point at which the simulation is desired; then the user can select the start of session range which is recorded and simulate forward in time until the simulation reaches the desired point so the post simulation analysis point is reached fast (CL42, L23-45). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with the system of **PA** that included write logic for writing state information at simulation time t0, because the user could select a particular point at which the simulation was desired; then the user could select the start of session range which was recorded and simulate forward in time until the simulation reached the desired point so the post simulation analysis point was reached fast.

Per Claim 15: **TA** teaches the process logic further comprises decompression logic for decompressing the compressed primary inputs (CL2, L29-31); and

data transfer logic for delivering the decompressed primary inputs to the hardware-modeled design for evaluation (CL1, L32-33; CL2, L31-33; Fig. 1, Blk17, 10 and 11).

7.3   As per Claim 19, **TA, LI** and **PA** teach the system of Claim 18. **TA** teaches access logic for accessing the VCD file directly from the beginning of the simulation target range to debug the modeled design (CL2, L56-61; CL5, L36-46); and

decompression logic for decompressing the compressed primary input data (CL2, L29-31) and delivering the decompressed primary input data into the modeled design for evaluation (CL1, L32-33; CL2, L31-33; Fig. 1, Blk17, 10 and 11).

TA, LI and **PA** do not expressly teach compression logic for receiving and compressing primary input data for the duration of the simulation session range. **MA** teaches compression logic for receiving and compressing primary input data for the duration of the simulation session range (Abstract, L12-15; CL5, L55 to CL6, L10), as the test pattern data after compression is stored in the memory (CL10, L54-56) and the memory required will be reduced by compression. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **TA, LI** and **PA** with the system of **MA** that included compression logic for receiving and compressing primary input data for the duration of the simulation session range, as the test pattern data after compression would be stored in the memory and the memory required would be reduced by compression.

Per Claim 20: **TA** teaches dump logic for dumping evaluated information to the VCD

file, the evaluated information generated by the evaluation of the decompressed primary inputs

by the modeled design (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44;

CL6, L21-25).

Conclusion

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from

8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for

the organization where this application or proceeding is assigned is 703-746-73210.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

9600.

K. Thangavelu
Art Unit 2123
September 2, 2003